REDUCING BUS WIDTH BY DATA COMPACTION

ABSTRACT

An integrated circuit device includes a processing component and a cache, which is arranged to store data for use by the processing component responsively to an addressing scheme based on memory addresses having an address length of m_1 bits. First and second buses are coupled between the processing component and the cache, the buses having bus widths of n_1 and n_2 bits, respectively, such that $n_1 < m_1$. The processing component and the cache each include a respective address bus expander coupled to the first bus in order to compact at least some of the memory addresses for transmission over the first bus so that each of the at least some memory addresses is transmitted over the first bus in one cycle of the first bus.